1. A method to optimize a signal routing in an integrated

circuit comprising:

providing a signal routing in an integrated circuit

layout wherein said signal routing comprises a

5   configuration of metal lines in a stack of metal levels and

wherein each said metal level is separated from an

underlying substrate by dielectric material

thereafter calculating a Joule heating estimate for

said signal routing;

10   thereafter comparing said Joule heating estimate to a

standard value;

thereafter updating said signal routing if said Joule

heating estimate exceeds said standard value wherein said

updating comprises generating a new configuration of said

15   metal lines in said metal levels and wherein said new

configuration reduces said Joule heating, and

thereafter repeating said steps of calculating,

comparing, and updating if said Joule heating estimate

still exceeds said standard value.

2. The method according to Claim 1 wherein said metal lines

comprise copper.

3. The method according to Claim 1 wherein said step of

updating said signal routing is performed by an automating routing system.

4. The method according to Claim 1 wherein said step of calculating a Joule heating estimate comprises a calculation based on current density in said metal lines and thermal conductivity of said dielectric material.

5. The method according to Claim 1 wherein said metal lines are formed by a damascene process.

6. The method according to Claim 1 wherein said step of updating said signal routing comprises reducing a total volume of said dielectric material between said metal lines and said substrate.

7. The method according to Claim 1 wherein said step of updating said signal routing comprises coupling said metal lines to a floating diffusion region in said substrate.

8. The method according to Claim 7 wherein said substrate comprises a p-type doping and said floating diffusion region comprises an n-type doping.

9. The method according to Claim 1 wherein said step of updating said signal routing comprises connecting said signal routing metal lines to a metal heat sink wherein said metal heat sink comprises a set of metal lines that

5   are connected together by vias to create a large thermal mass.

10. The method according to Claim 9 wherein said set of metal lines are formed in metal levels lower than said signal routing metal lines.

11. A method to design an integrated circuit device comprising:

generating an integrated circuit layout comprising a plurality circuit elements and signal nodes and

5   comprising a stack of metal levels defining a plurality of signal routings between said signal nodes wherein each said signal routing comprises a configuration of metal lines in said metal levels and wherein each said metal level is separated from an underlying substrate by dielectric

10   material;

thereafter calculating Joule heating estimates for each said signal routing;

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thereafter comparing said signal routing Joule heating

estimates to a standard value; and

15   thereafter updating said signal routings for each said

signal routing where said Joule heating estimate exceeds

said standard value wherein said updating comprises

generating a new configuration of metal lines in said metal

levels and wherein said new configurations reduce Joule

20   heating in said signal routings; and

thereafter repeating said steps of calculating,

comparing, and updating until all of said Joule heating

estimates do not exceed said standard value.

12. The method according to Claim 11 wherein said metal

lines comprise copper.

13. The method according to Claim 11 wherein said steps of

generating an integrated circuit layout and of updating

said signal routings are performed by an automating routing

system.

14. The method according to Claim 11 wherein said step of

calculating Joule heating estimates comprises a calculation

based on current density in said metal lines and thermal

conductivity of said dielectric material.

15. The method according to Claim 11 wherein said metal lines are formed by a damascene process.

16. The method according to Claim 11 wherein said step of updating said signal routings comprises reducing total volumes of said dielectric material between said metal lines and said substrate.

17. The method according to Claim 11 wherein said step of updating said signal routings comprises coupling said metal lines to a floating diffusion region in said substrate.

18. The method according to Claim 17 wherein said substrate comprises a p-type doping and said floating diffusion region comprises an n-type doping.

19. The method according to Claim 11 wherein said step of updating said signal routing comprises connecting said signal routing metal lines to a metal heat sink wherein said metal heat sink comprises a set of metal lines that 5 are connected together by vias to create a large thermal mass.

20. The method according to Claim 19 wherein said set of metal lines are formed in metal levels lower than said signal routing metal lines.

21. A signal routing structure in an integrated circuit comprising:

    a first set of metal lines in a stack of metal levels wherein each said metal level is separated from an

5   underlying substrate by dielectric material; and

    a heat sink coupled to said first set of metal lines by a via or numbers of vias.

22. The structure according to Claim 21 wherein said heat sink comprises a second set of metal lines that are connected together by vias to create a large thermal mass.

23. The method according to Claim 22 wherein said second set of metal lines are formed in metal levels lower than said first set of metal lines.

24. The structure according to Claim 21 wherein said heat sink comprises a floating diffusion region in said substrate.

25. The structure according to Claim 24 wherein

said substrate comprises a p-type doping and said floating

diffusion region comprises an n-type doping.